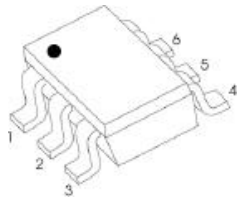
Dual Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

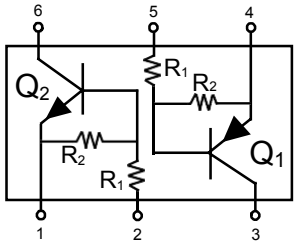
MMUN5311DW Series

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base–emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the MMUN5311DWseries, two complementary BRT devices are housed in the SOT–363 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- We declare that the material of product compliance with RoHS requirements.



SOT-363



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, – minus sign for Q_1 (PNP) omitted)

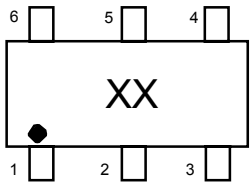
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C	P_D	187 (Note 1.) 256 (Note 2.)	mW
Derate above 25°C		1.5 (Note 1.) 2.0 (Note 2.)	mW/°C
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	670 (Note 1.) 490 (Note 2.)	°C/W
Characteristic (Both Junctions Heated)	**Symbol**	**Max**	**Unit**
Total Device Dissipation T_A = 25°C	P_D	250 (Note 1.) 385 (Note 2.)	mW
Derate above 25°C		2.0 (Note 1.) 3.0 (Note 2.)	mW/°C
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	493 (Note 1.) 325 (Note 2.)	°C/W
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	188 (Note 1.) 208 (Note 2.)	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

1. FR–4 @ Minimum Pad 2. FR–4 @ 1.0 x 1.0 inch Pad

MARKING DIAGRAM



xx = Device Marking
(See Page 2)

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

ORDERING, SHIPPING, DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1(K)	R2(K)	Shipping
MMUN5311DW	SOT-363	11	10	10	3000/Tape&Reel
MMUN5312DW	SOT-363	12	22	22	3000/Tape&Reel
MMUN5313DW	SOT-363	13	47	47	3000/Tape&Reel
MMUN5314DW	SOT-363	14	10	47	3000/Tape&Reel
MMUN5315DW	SOT-363	15	10	Ğ	3000/Tape&Reel
MMUN5316DW	SOT-363	16	4.7	Ğ	3000/Tape&Reel
MMUN5330DW	SOT-363	30	1	1	3000/Tape&Reel
MMUN5331DW	SOT-363	31	2.2	2.2	3000/Tape&Reel
MMUN5332DW	SOT-363	32	4.7	4.7	3000/Tape&Reel
MMUN5333DW	SOT-363	33	4.7	47	3000/Tape&Reel
MMUN5334DW	SOT-363	34	22	47	3000/Tape&Reel
MMUN5335DW	SOT-363	35	2.2	47	3000/Tape&Reel

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q_1 (PNP) omitted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 4)						
DC Current Gain (V_{CE} = 10 V, I_C = 5.0 mA)	MMUN5311DW	h_{FE}	35	60	−	
	MMUN5312DW		60	100	−	
	MMUN5313DW		80	140	−	
	MMUN5314DW		80	140	−	
	MMUN5315DW		160	350	−	
	MMUN5316DW		160	350	−	
	MMUN5330DW		3.0	5.0	−	
	MMUN5331DW		8.0	15	−	
	MMUN5332DW		15	30	−	
	MMUN5333DW		80	200	−	
	MMUN5334DW		80	150	−	
	MMUN5335DW		80	140	−	
Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA) (I_C = 10 mA, I_B = 5 mA) MMUN5330DW /MMUN5331DW (I_C = 10 mA, I_B = 1 mA) LMUN5315DW/MMUN5316DW MMUN5332DW /MMUN5333DW /MMUN5334DW		$V_{CE(sat)}$	−	−	0.25	Vdc
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kfi)	MMUN5311DW		−	−	0.2	
	MMUN5312DW		−	−	0.2	
	MMUN5314DW		−	−	0.2	
	MMUN5315DW		−	−	0.2	
	MMUN5316DW		−	−	0.2	
	MMUN5330DW		−	−	0.2	
	MMUN5331DW		−	−	0.2	
	MMUN5332DW		−	−	0.2	
	MMUN5333DW		−	−	0.2	
	MMUN5334DW		−	−	0.2	
	MMUN5335DW		−	−	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kfi)	MMUN5313DW		−	−	0.2	
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kfi) (V_{CC} = 5.0 V, V_B = 0.050 V, R_L = 1.0 kfi) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kfi)	MMUN5330DW MMUN5315DW MMUN5316DW MMUN5333DW	V_{OH}	4.9	−	−	Vdc
Input Resistor	MMUN5311DW	R1	7.0	10	13	k fi
	MMUN5312DW		15.4	22	28.6	
	MMUN5313DW		32.9	47	61.1	
	MMUN5314DW		7.0	10	13	
	MMUN5315DW		7.0	10	13	
	MMUN5316DW		3.3	4.7	6.1	
	MMUN5330DW		0.7	1.0	1.3	
	MMUN5331DW		1.5	2.2	2.9	
	MMUN5332DW		3.3	4.7	6.1	
	MMUN5333DW		3.3	4.7	6.1	
	MMUN5334DW		15.4	22	28.6	
	MMUN5335DW		1.54	2.2	2.86	
Resistor Ratio	MMUN5311DW /MMUN5312DW1 /MMUN5313DW	R1/R2	0.8	1.0	1.2	
	MMUN5314DW		0.17	0.21	0.25	
	MMUN5315DW /LMUN5316DW		−	−	−	
	MMUN5330DW /MMUN5331DW /MMUN5332DW		0.8	1.0	1.2	
	MMUN5333DW		0.055	0.1	0.185	
	MMUN5334DW		0.38	0.47	0.56	
	MMUN5335DW		0.038	0.047	0.056	

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted, common for Q_1 and Q_2, − minus sign for Q_1 (PNP) omitted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	MMUN5311DW	I_{EBO}	–	–	0.5	mAdc
	MMUN5312DW		–	–	0.2	
	MMUN5313DW		–	–	0.1	
	MMUN5314DW		–	–	0.2	
	MMUN5315DW		–	–	0.9	
	MMUN5316DW		–	–	1.9	
	MMUN5330DW		–	–	4.3	
	MMUN5331DW		–	–	2.3	
	MMUN5332DW		–	–	1.5	
	MMUN5333DW		–	–	0.18	
	MMUN5334DW		–	–	0.13	
	MMUN5335DW		–	–	0.2	
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	–	–	Vdc

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ALL MMUN5311DW1T1G SERIES DEVICES

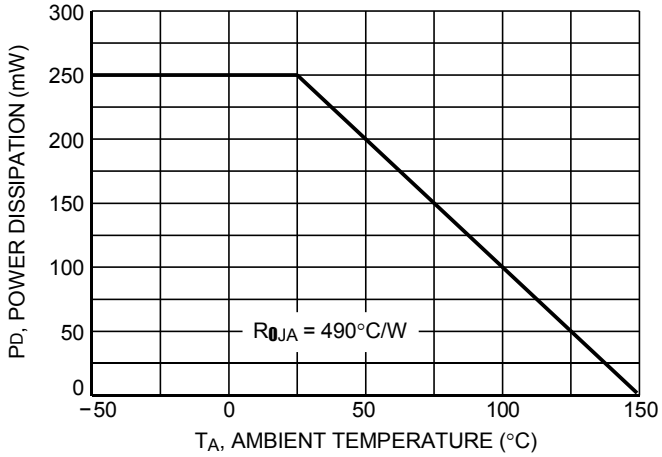


Figure 1. Derating Curve

TYPICAL ELECTRICAL CHARACTERISTICS − MMUN5311DW NPN TRANSISTOR

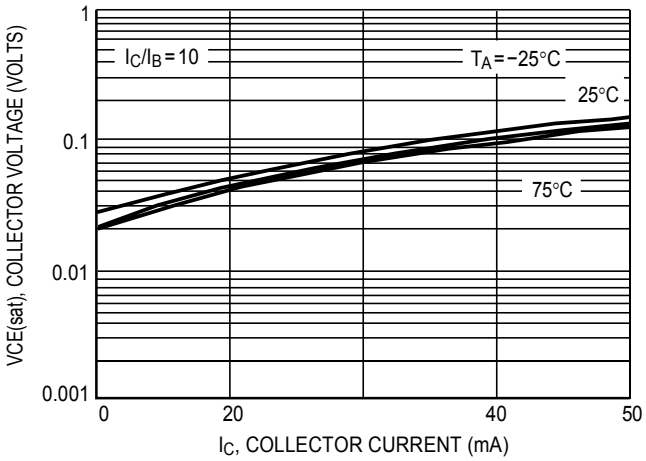


Figure 2. $V_{CE(sat)}$ versus I_C

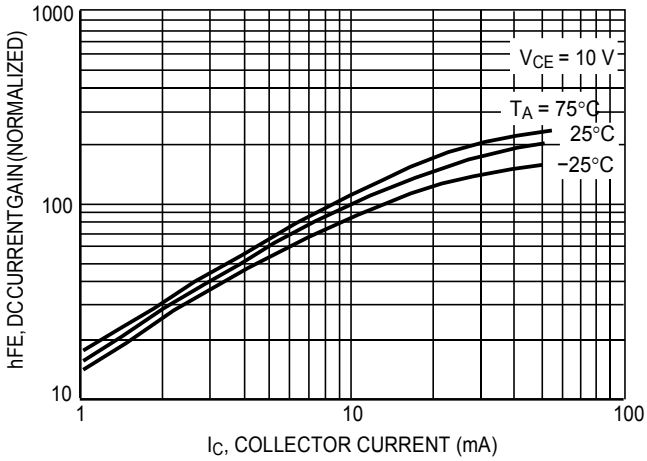


Figure 3. DC Current Gain

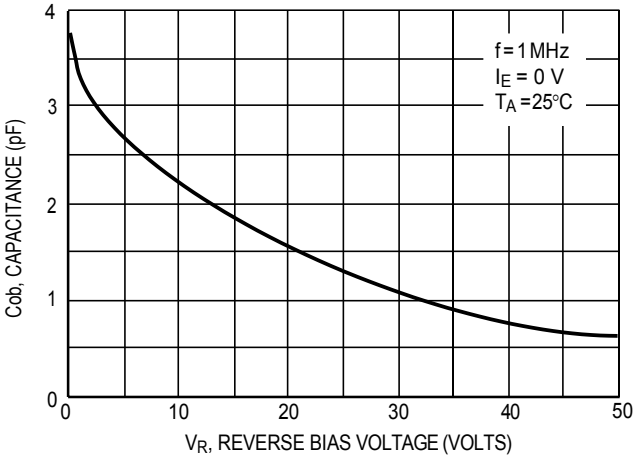


Figure 4. Output Capacitance

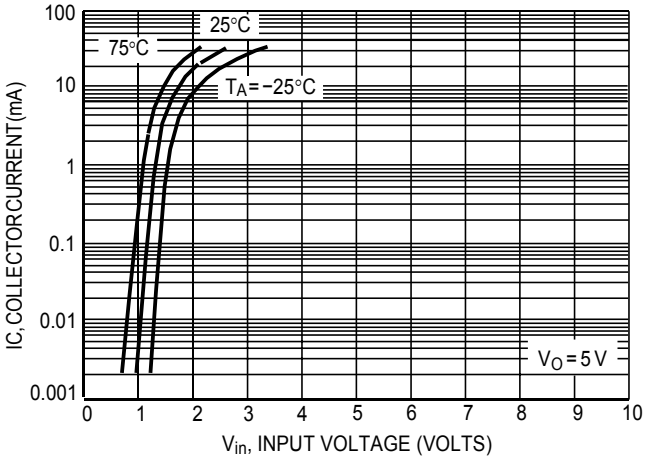


Figure 5. Output Current versus Input Voltage

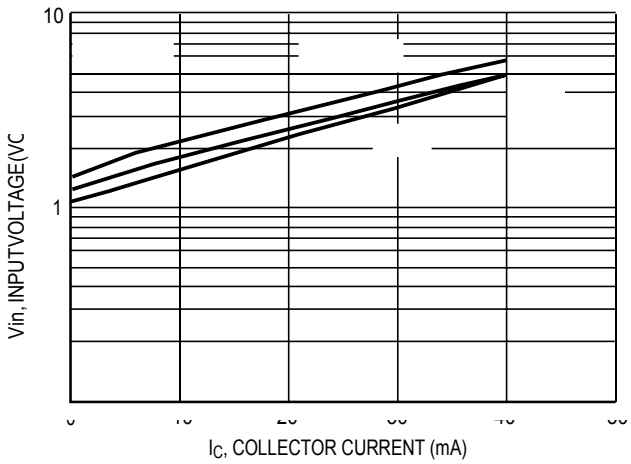


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS − MMUN5311DW PNP TRANSISTOR

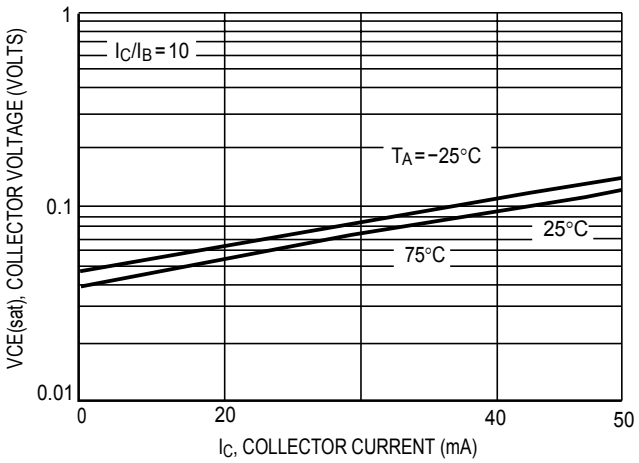


Figure 7. $V_{CE(sat)}$ versus I_C

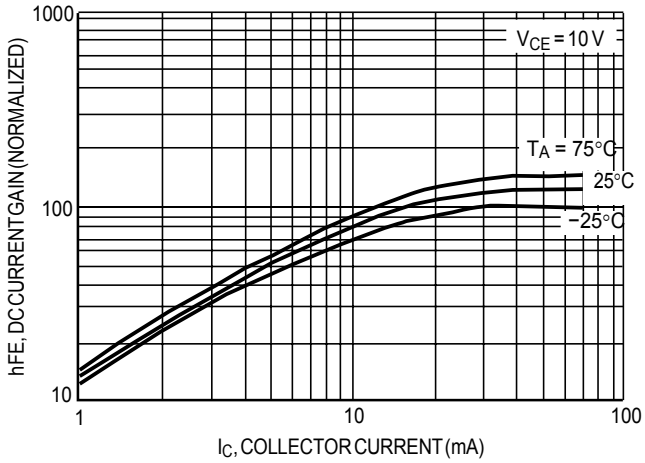


Figure 8. DC Current Gain

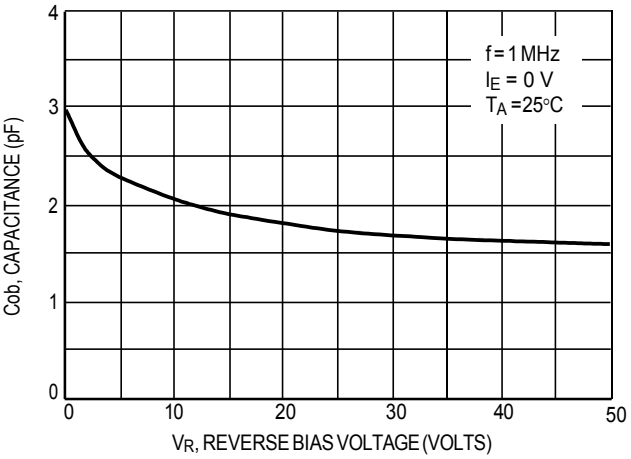


Figure 9. Output Capacitance

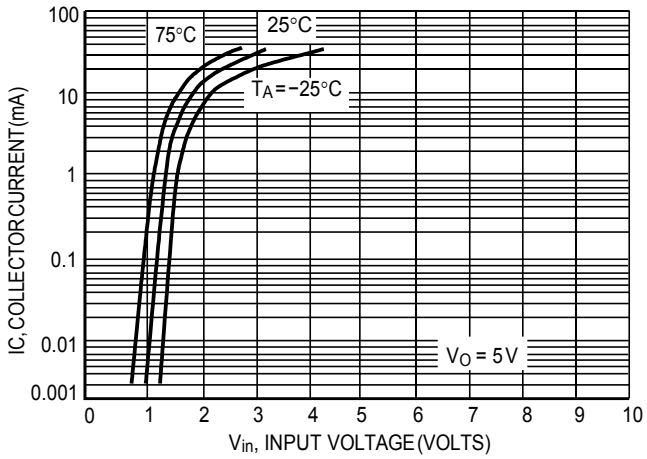


Figure 10. Output Current versus Input Voltage

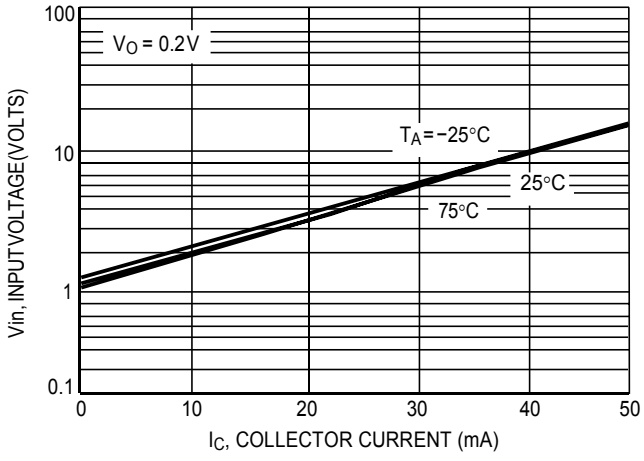


Figure 11. Input Voltage versus Output Current